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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,335	12/14/2006	Katsuki Kusunoki	Q79257	6238

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EXAMINER	
PATHAK, SHANTANU	
ART UNIT	PAPER NUMBER
4126	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,335	KUSUNOKI, KATSUKI	
	Examiner	Art Unit	
	SHANTANU PATHAK	4126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/02/2006, 12/14/2006, 10/05/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-7, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji et al. (Japan Patent No. JP10125958) in view of Araghi (US Patent No. 4,604,161).

With respect to Claims 1, 6 and 7, Shuji et al. (Japan Patent No. JP10125958), hereinafter referred to as "Shuji", teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate, comprising: a step of linearly forming first grooves (11) in a desired chip shape by etching on a side of the gallium nitride compound semiconductor layers (2, 3) of said wafer (Paragraph 7, lines 1-6; Drawing 3, elements 11, 2, 3) and a step of dividing said wafer along said first and second grooves into pieces each of a chip shape (Paragraph 7, lines 11, 12; Paragraph 10, lines 12-14; Paragraph 21, lines 9, 10) {Examiner's interpretation: The wafers are separated along the "Chuo Line"} **[Claim 1]**. Shuji further teaches the limitations wherein said first grooves are confronted by an electrode-forming surface for forming an electrode for gallium nitride compound semiconductor chips (Paragraph 16, lines 3-6) {Examiner's interpretation: First grooves are formed in material layers comprising

gallium nitride layer 3 over which an electrode-forming surface can be formed. If the electrode-forming surface is formed over gallium nitride layer 3, then the first grooves will be formed in material layers comprising the electrode-forming surface} **[Claim 6]** and wherein said second grooves are formed by at least one method selected from the group consisting of etching, dicing, pulse laser and scriber (Paragraph 9, lines 1-3) **[Claim 7]**.

While Shuji does not explicitly disclose a step of forming second grooves (22) having a nearly equal or smaller line width (W2) than a line width (W1) of the first grooves on a side of the substrate (1) of said wafer at positions not conforming to the central lines of the first grooves, Shuji does disclose a step of forming second grooves (22) having a nearly equal or smaller line width (W2) than a line width (W1) of the first grooves on a side of the substrate (1) of said wafer (Paragraph 7, lines 9, 10; Drawing 3, elements W1, 11, W2, 22) **[Claim 1]**.

Araghi (US Patent No. 4,604,161), hereinafter referred to as "Araghi", teaches a method of fabricating image sensor arrays for assembly with other like arrays to form a longer composite array without sacrifice of image quality. Araghi further discloses a step of forming second grooves…of said wafer at positions not conforming to the central lines of the first grooves (Column 3, lines 50-56; Fig. 3, elements 35, 37, 40, 44, 45) **[Claim 1]**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji with the groove positioning as taught by Araghi to provide chips having precisely controlled ends and line edges for butting against the ends of like arrays (Araghi).

With respect to Claims 3-5, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound

semiconductor layers laminated on a principal surface of a substrate as described in Claim 1. Shuji in view of Araghi does not explicitly disclose the limitations wherein the positions not confirming to the central lines of said first grooves are, when viewing the substrate in plan[e] view, positions parted by 20 to 100% of the line width (W1) of the first grooves relative to the central lines of the first grooves **[Claim 3]** and wherein at the step of forming said second grooves, the second grooves are formed so that the obliquely divided chips assume cut faces having angles in the range of 60 to 85° **[Claim 4]** or the step of polishing the substrate side prior to forming the second grooves to adjust a thickness of the substrate in a range of 60 to 100 μm **[Claim 5]**. It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the limitations as described in Claims 3-5 of the instant application in the invention of Shuji in view of Araghi because "[w]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)

With respect to Claim 11, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate as described in Claim 1. That the final product resultant from a method for the production of gallium nitride compound semiconductor chips is a gallium nitride compound semiconductor chip is inherent to the process.

3. Claims 1, 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji et al. (Japan Patent No. JP10125958) in view of Araghi (US Patent No. 4,604,161) as applied to claim 1 above, and further in view of Tsuda et al. (US PG Pub No. 2002/0014681 A1).

With respect to Claim 2, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate as described in Claim 1. However, Shuji in view of Araghi does not disclose the limitation wherein said substrate is formed of sapphire, with a C surface of the sapphire substrate as the principal surface, said first and second grooves are formed respectively along a first direction parallel to an orientation fiat (11-20) and along a second direction orthogonal to said first direction, and the wafer is divided along the first and second grooves.

Tsuda et al. (US PG Pub No. 2002/0014681 A1), hereinafter referred to as "Tsuda", teaches a method of producing a nitride semiconductor structure for employing in light-emitting devices. Tsuda further discloses the limitation wherein said substrate is formed of sapphire, with a C surface of the sapphire substrate as the principal surface, said first and second grooves are formed respectively along a first direction parallel to an orientation fiat (11-20) and along a second direction orthogonal to said first direction, and the wafer is divided along the first and second grooves (Paragraph 45: definitions of "groove" and "cleavage direction"; Paragraphs 56, 57) {Examiner's interpretation: (1) The C plane of the sapphire substrate is the principle surface, (2) Grooves are formed parallel to the [11-20] plane, and (3) Since the gallium nitride semiconductor is formed along the [11-20] plane, grooves formed perpendicular to the lateral

growth of the gallium nitride semiconductor means the grooves also are perpendicular to the [11-20] plane}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shuji in view of Araghi with the groove directionality as taught by Tsuda to prevent cracks and improve the crystal quality of the nitride semiconductor film.

4. Claims 1, 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuji et al. (Japan Patent No. JP10125958) in view of Araghi (US Patent No. 4,604,161) as applied to claim 1 above, and further in view of Tanaka et al. (US PG Pub No. 2001/0038655 A1).

With respect to Claims 8-10, Shuji in view of Araghi teaches a method for the production of gallium nitride compound semiconductor chips from a wafer having gallium nitride compound semiconductor layers laminated on a principal surface of a substrate as described in Claim 1. While Shuji in view of Araghi does not disclose the limitations wherein said substrate is formed of hexagonal SiC **[Claim 8]**, said substrate is formed of a hexagonal nitride semiconductor **[Claim 9]**, or said substrate is formed of hexagonal GaN **[Claim 10]**, the limitations as disclosed in Claims 8-10 are considered as obvious variants.

Tanaka et al. (US PG Pub No. 2001/0038655 A1), hereinafter referred to as "Tanaka", teaches a method of crystal growth of a III-V compound semiconductor composed of at least one group-III element, with the crystal being hexagonal in structure or a nitride semiconductor. Tanaka further discloses the similarities in crystal structure between sapphire and hexagonal SiC (Paragraph 138) **[Claim 8]**, hexagonal nitride semiconductor (Paragraph 19, lines 11-14) **[Claim 9]** and hexagonal GaN (Paragraph 19, lines 1-10) **[Claim 10]**. Therefore, it would have been

obvious to one of ordinary skill in the art at the time of the invention to modify Shuji in view of Araghi with the material surfaces as taught by Tanaka to understand crystal growth mechanisms of III-V compound layers for use in semiconductor device applications.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oohata (US Patent No. 6,963,086 B2), Tanabe et al. (US Patent No. 6,680,959 B2) and Tanabe et al. (US Patent No. 6,735,230 B1) are all related to the manufacture of semiconductor light-emitting devices comprising gallium nitride chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHANTANU PATHAK whose telephone number is (571)270-5727. The examiner can normally be reached on Monday-Thursday, 10:00 a.m.-4:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tu Nguyen can be reached on 571-272-2424. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. P./
Examiner, Art Unit 4126

/James P. Hughes/
Primary Examiner, Art Unit 2883